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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TUCKER, WESLEY J	

ART UNIT	PAPER NUMBER
2624	

DATE MAILED: 04/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/749,819	FUKUDA ET AL.	
	Examiner	Art Unit	
	Wes Tucker	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6,8-11 and 13-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,8-11 and 13-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 7th, 2006 has been entered.

Response to Amendments and Arguments

2. Applicant's response to the last Office Action, filed April, 7th 2006, has been entered and made of record.

3. Applicant has amended claims 1, 3-6, 8-11, and 13-16. Claims 2, 7 and 12 are cancelled. Claims 1, 3-6, 8-11 and 13-20 are pending.

4. Applicant's arguments have been fully considered but are not persuasive for at least the following reasons:

5. Applicant has amended the independent claims to include the newly added features listed as follows:

a memory controller section configured to be responsive to the control register section outputs to control selection of one data transfer mode from a plurality of data transfer modes available to provide different data transfer

operations between the arithmetic processing unit and the memory, said transfer modes including at least a random access transfer mode in which a memory address must be included to access the memory for said data transfer and at least one other data transfer mode.

Effectively, applicant has added the limitation of selecting a data transfer mode in order to distinguish from the prior art.

The reference of U.S. Patent 4,841,435 to Papenburg teaches that a transfer mode is determined and information is sent to a controller in order to effect a certain kind of data transfer information (column 16, lines 25-47). Papenburg teaches that the transfer mode, either random or block, is chosen according to the efficiency of the type of transfer for a certain subset of data. Therefore it would have been obvious to one of ordinary skill in the art to enable different transfer modes including a random transfer mode as taught by Papenburg to enable more efficient data transfer according to the kind of data to be transferred. A new rejection under 35 USC 103 has been presented below.

Also in view of the now presented amendment a 35 USC 101 rejection has been made on all of the claims below.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-3, 6-8, 11-13, and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of U.S. Patents 5,355,508 to Kan and 6,704,456 to Venable and 4,841,435 to Papenburg.

With regard to claim 1, Kan discloses an image processing apparatus configured to receive image data (column 7, lines 45-50), an arithmetic processing unit configured to process said image data relating to said image data received (Fig. 2, element 108) to provide processed image data representing a reproduction of the image, said processing unit including:

A programmable arithmetic processing section of SIMD (Single Instruction Multiple Data Stream) type configured to provide simultaneous processing of plural image data portions (Figs. 1, 2, and 4 and column 6, lines 24-30 and column 6, lines 36-51). Kan teaches that the SIMD is used in the image processing field and is used to effect faster processing on each block of data. Data blocks are interpreted in the field of image processing as image portions.

Kan further discloses a memory configured with a plurality of addressable memory locations, with each memory location storing image data portions relating to image data portions relating to the image data received (Fig. 2, elements 42 and 98-101).

Kan discloses a control register section (Fig. 2, element 11) configured to receive control inputs directly from a control unit (Figs. 1 and 2, element 43), said control unit (43) being outside of said arithmetic processing unit (50), said control register section being further configured to provide control register section outputs based on said control inputs (Fig. 2, elements 11, 103 and 102), and

a memory controller section (103) configured to be responsive to the control register section (11) outputs to control access to at least some of addressable memory locations...

Kan discloses a system controller (11), which is interpreted as a control register section. It is a controller and is interpreted to inherently contain a register as a register is defined as the part of a processor used for storage. A controller must inherently contain a register of some form with which to process digital information.

Kan discloses that the control register or system controller is configured to receive control inputs directly from a control unit (43). The control unit (43) appears to be in direct connection with in direct connection with the control register section (11) as seen in both figures 1 and 2 and therefore it is reasonably assumed that the control register (11) receives inputs directly from the control unit (43).

It is also clear from the figures 1 and 2 in Kan that the control unit is outside of said arithmetic processing unit (50).

It is also reasonably assumed that said control register section is configured to provide control register section outputs based on said control inputs (Fig. 2, elements 11, 103 and 102). In the Figures 1 and 2 disclosed in Kan, there is an outside controller

43 configured with a control register or system controller 11. What is now being claimed in this particular passage is the most basic and elementary of computer operations involving outputting signals from one controller based on inputting signals from another controller. It is reasonably assumed that the two controllers disclosed in Kan operate in this manner as this is how all computer registers/controllers work and why controllers are termed controllers, because they affect and dictate the input/output of other circuitry.

Kan further discloses a memory controller (103) configured to be responsive to the control register section (11) outputs to control access to at least some of the memory locations... The same discussion presented above with regard to controller operation applies here (column 6, lines 34-42).

Kan further discloses a memory controller section configured to access at least some of said addressable memory locations to control transfer of the image data portions stored thereat to said programmable arithmetic processing section depending on types of said simultaneous processing to provide said plural image data portions undergoing said simultaneous processing to provide said processing to provide said processing image data representing the reproduction of said original document (Fig. 2, element 103 and column 6, lines 38-51). Here the input controller 103 is interpreted as a memory controller as the input controller allows access to memory locations and distributes data to the arithmetic processing section 108.

Kan does not disclose the feature of an image unit configured to provide image data based on a scanned original document. The use of scanners, printers, and the like

are exceedingly well known in the art. It is common practice to scan image data and then perform image processing on that image data, just as it is common practice to output a processed image to a monitor or printer or any acceptable output device. Venable discloses a scanner (column 5, lines 60-68) which inherently contains a sensor board arranged to receive image data based on a scanned original document. Venable teaches that image processing is performed on the input image and also discloses a printer (column 5, lines 60-68), which is interpreted as an image writing unit arranged to transfer said reproduction of said original document to a second document. Venable discloses a scanner for scanning images and then performing some kind of image processing and then printing the finished image on a printer (column 5, lines 60-68). The motivation to combine the two references of Venable and Kan is the same that would motivate anyone skilled in the art to input or output a processed image. An image must be input to the processor disclosed by Kan and the processed image must be output in some form in order to show or appreciate the results obtained from that processing. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use a scanner and a printer as taught by Venable and as is well known in the art to input and output data to and from the processor disclosed by Kan.

Kan and Venable do not disclose explicitly disclose the newly amended features listed as follows:

a memory controller section configured to be responsive to the control register section outputs to control selection of one data transfer mode from a

plurality of data transfer modes available to provide different data transfer operations between the arithmetic processing unit and the memory, said transfer modes including at least a random access transfer mode in which a memory address must be included to access the memory for said data transfer and at least one other data transfer mode.

Kan discloses the image processing apparatus according to claim 1, wherein said control register section (11) is configured to provide a control register section output to the memory controller section (103) to provide a data transfer mode setting function for setting a data transfer mode of the addressable memory locations accessed by the memory controller section (column 6, lines 34-42). The system controller 11 is interpreted as a control register section as the system controller issues instructions to the memory controller (input controller 103) in order to transfer data from the memory 42 to the arithmetic processing unit 108. This is interpreted as setting the transfer mode as the transfer is determined by the system controller and the input controller. Kan also discloses the controller to have the capability of performing both random memory access and automatic memory access. The controller manages parallel processing and memory access and performs both neighborhood processing in which the memory location must be set to locate the potion of the image to be processed and general processing in which processing of the entire image occurs and the memory address is read automatically.

However Kan does not explicitly disclose the determination of a data transfer mode.

Papenburg teaches that a transfer mode is determined and information is sent to a controller in order to use a certain kind of data transfer information (column 16, lines 25-47). Papenburg teaches that the transfer mode, either random or block, is chosen according to the efficiency of the type of transfer for a certain subset of data. Furthermore the memory address must be included when performing a random access transfer of data. Therefore it would have been obvious to one of ordinary skill in the art to enable different transfer modes including a random transfer mode as taught by Papenburg to enable more efficient data transfer according to the kind of data to be transferred.

With regard to claim 3, Kan, Venable and Papenburg disclose the image processing apparatus according to claim 2, and Kan discloses the controller to have the capability of performing both random memory access and automatic memory access. The controller manages parallel processing and memory access and performs both neighborhood processing in which the memory location must be set to locate the potion of the image to be processed and general processing in which processing of the entire image occurs and the memory address is read automatically (column 8, lines 62-67 and column 9, lines 1-13). However Kan does not explicitly disclose the determining between either random or automatic transfer mode, so Papenburg has been cited to teach such a determination in data transfer operations.

Papenburg discloses wherein said at least one other data transfer mode is an automatic access mode in which an address is automatically updated to access the

memory. Papenburg teaches that a transfer mode is determined and information is sent to a controller in order to use a certain kind of data transfer information (column 16, lines 25-47). Papenburg teaches that the transfer mode, either random or block, is chosen according to the efficiency of the type of transfer for a certain subset of data. The block mode is interpreted as the automatic data transfer mode. Therefore it would have been obvious to one of ordinary skill in the art to enable different transfer modes including a random transfer mode as taught by Papenburg to enable more efficient data transfer according to the kind of data to be transferred.

Claims 6, 7 and 8 are similar to claims 1, 2 and 3 except that 6, 7 and 8 make reference to means. It is understood that the means are included in the elements such as registers, controllers, units, etc. Therefore the discussions of claims 1, 2 and 3 apply for claims 6, 7 and 8.

Claims 11, 12 and 13 are similar to claims 1, 2 and 3 except that 11, 12 and 13 make reference to method. It is understood that the intended method is included in the apparatus claimed in claims 1, 2 and 3. Therefore the discussions of claims 1, 2 and 3 apply for claims 11, 12 and 13.

With regard to claim 16, Kan discloses a computer readable medium for storing instructions, which when executed by a computer, causes the computer to perform an image processing method to be executed by an image processing apparatus, said

image processing apparatus including a programmable SIMD type arithmetic image processing section for simultaneous processing a plurality of image data portions (Fig. 2 and column 6, lines 14-30), each image data portion being digital signals prepared based on an input image (column 7, lines 45-50) and a memory having a plurality of addressable memory locations (Fig. 2, element 42) accessible by a memory controller section (Fig. 2, element 103) to provide image data stored at said plurality of addressable memory locations as image data portions related to the image to said arithmetic processing section (Fig. 2, element 108) as said plurality of image data portions for simultaneous processing (column 6, lines 35-38) , the method comprising steps of:

receiving control inputs directly from a control unit (43) at a control register section (11), said control unit being external to said arithmetic processing section (Figs. 1 and 2).

Processing said control inputs at said control register (11) section to provide control register section outputs to said memory controller (103) section (column 6, lines 34-45).

controlling transfer of at least some of the image data portions relating to the document image data between said addressable memory locations (Fig. 2, element 42) and said arithmetic processing section (Fig. 2, element 108), by using said memory controller section under control of the control register section outputs (Fig. 2, element 103) and controlling transfer of processed data from said programmable arithmetic processing section to provide a processed reproduction of said document image

(column 6, lines 35-50). Here the input controller 103 is interpreted as a memory controller as the input controller allows access to memory locations 42 and distributes data to the arithmetic processing section 108.

Kan does not disclose the feature a sensor board arranged to receive image data based on a scanned document or an image writing unit arranged to receive and use processed image data representing the reproduction of said original document to produce a second image document. The use of scanners, printers, and the like are exceedingly well known in the art. It is common practice to scan image data and then perform image processing on that image data, just as it is common practice to output a processed image to a monitor or printer or any acceptable output device. Venable discloses a scanner (column 5, lines 60-68) which inherently contains a sensor board arranged to receive image data based on a scanned original document. Venable teaches that image processing is performed on the input image and also discloses a printer (column 5, lines 60-68), which is interpreted as an image writing unit arranged to transfer said reproduction of said original document to a second document. Venable discloses a scanner for scanning images and then performing some kind of image processing and then printing the finished image on a printer (column 5, lines 60-68). The motivation to combine the two references of Venable and Kan is the same that would motivate anyone skilled in the art to input or output a processed image. An image must be input to the processor disclosed by Kan and the processed image must be output in some form in order to show or appreciate the results obtained from that processing. Therefore it would have been obvious to one of ordinary skill in the art at

the time of invention to use a scanner and a printer as taught by Venable and as is well known in the art to input and output data to and from the processor disclosed by Kan.

Kan and Venable do not disclose explicitly disclose the newly amended features listed as follows:

a memory controller section configured to be responsive to the control register section outputs to control selection of one data transfer mode from a plurality of data transfer modes available to provide different data transfer operations between the arithmetic processing unit and the memory, said transfer modes including at least a random access transfer mode in which a memory address must be included to access the memory for said data transfer and at least one other data transfer mode.

Kan discloses the image processing apparatus according to claim 1, wherein said control register section (11) is configured to provide a control register section output to the memory controller section (103) to provide a data transfer mode setting function for setting a data transfer mode of the addressable memory locations accessed by the memory controller section (column 6, lines 34-42). The system controller 11 is interpreted as a control register section as the system controller issues instructions to the memory controller (input controller 103) in order to transfer data from the memory 42 to the arithmetic processing unit 108. This is interpreted as setting the transfer mode as the transfer is determined by the system controller and the input controller. Kan also discloses the controller to have the capability of performing both random memory access and automatic memory access. The controller manages parallel processing and

memory access and performs both neighborhood processing in which the memory location must be set to locate the potion of the image to be processed and general processing in which processing of the entire image occurs and the memory address is read automatically.

However Kan does not explicitly disclose the determination of a data transfer mode.

Papenburg teaches that a transfer mode is determined and information is sent to a controller in order to use a certain kind of data transfer information (column 16, lines 25-47). Papenburg teaches that the transfer mode, either random or block, is chosen according to the efficiency of the type of transfer for a certain subset of data. Furthermore the memory address must be included when performing a random access transfer of data. Therefore it would have been obvious to one of ordinary skill in the art to enable different transfer modes including a random transfer mode as taught by Papenburg to enable more efficient data transfer according to the kind of data to be transferred.

With regard to claim 17, Kan and Venable disclose the image processing apparatus according to claim 1, and Kan further discloses comprising an image data control unit arranged to expand an image are[a] of said image data (column 2, lines 26-44). Kan discloses performing geometric transformations, which is interpreted to mean expanding an image area.

With regard to claim 18, Kan and Venable disclose the image processing apparatus according to claim 17, but do not explicitly disclose wherein said image data control unit is arranged to scale said image data, however scaling images is well known in the art and Examiner takes official notice.

With regard to claim 19, Kan and Venable disclose the image processing apparatus according to claim 17 and Kan further discloses wherein said image data control unit is arranged to synthesize a plurality of sets of image data (column 6, lines 40-45). The different image data blocks are processed and then sent back to locations in the segmented memory so the data control unit (Fig. 2, element 11) must be inherently configured to synthesize a plurality of sets of image data as image data is divided among a plurality of memories and processors.

With regard to claim 20, Kan and Venable disclose the image processing apparatus according to claim 19, and Venable discloses wherein at least one of said plurality of sets of image data is communicated to said image processing apparatus from another apparatus (column 5, lines 64-68). Here Venable discloses images that can be stored in memory, printed, or transferred via network.

8. Claims 4, 9, and 14 rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of U.S. Patents 5,355,508 to Kan and 6,704,456 to

Venable and 4,841,435 to Papenburg and further in view of U.S. Patent 6,023,746 to Arimilli et al.

With regard to claim 4, Kan and Venable and Papenburg disclose the method of claim 2, but do not disclose wherein said at least one other data transfer mode is a redundant transfer mode in which data is transferred redundantly from a single asdressable memory location of said memory to a plurality of processing elements in said arithmetic processing section.

Arimilli discloses reading data redundantly from a cache directory using a redundant address index in a cache. Arimilli teaches that if an error occurs when reading the address from the first cache that the address is read from the second address location. This is interpreted to read on the claimed features of claim 4, because the data is read from redundantly from two address lines, which reference the same memory location for reading data out. Arimilli teaches that the redundant reading is done as a way to avoid an addressing error fro reading out data to be processed. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use the redundant reading method of Arimilli in combination with the memory configuration taught by Kan in order to avoid addressing errors in reading from multiple memory locations in performing parallel processing.

With regard to claims 9 and 14, the discussion of claim 4 applies.

9. Claims 5,10, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of U.S. Patents 5,355,508 to Kan and U.S. Patent 6,704,456 to Venable and 4,841,435 to Papenburg and further in view of U.S. Patent 6,229,954 to Yamagami et al.

With regard to claim 5, Kan and Venable and Papenburg disclose the image processing apparatus according to claim 2, but does not disclose the apparatus wherein said control register reads data from said arithmetic processing section by thinning out, in accordance with a control signal provided from outside, and sets a thinning-out read transfer mode for transferring data to said memory. Yamagami discloses a thinning out process (column 4, lines 15-25). Here a thinning-out process circuit (Fig.2, element 204) is disclosed and is controlled by the bus controller (Fig.2, element 206) which controls the data transfer between memory and the thinning out circuit and is therefore the memory control. The bus controller receives an outside signal from the External I/F Controller (Fig.2, element 207) and sets the data transfer to thinning-out. Thinning-out of data in a digital image environment is useful because memory is limited and digital images contain a relatively large amount of data. Any thinning out or minimization of data needed to represent the digital image will result in more available memory to be used. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use the thinning out technique of Yamagami in order to better utilize limited memory in the environment of digital imaging.

With regard to claims 10 and 15, the discussion of claim 5 applies.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wes Tucker whose telephone number is 571-272-7427. The examiner can normally be reached on 9AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bhavesh Mehta can be reached on 571-272-2214. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Wes Tucker

4-17-05

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